REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated October 23, 2006. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 23-25 are under consideration in this application. Claims 2-13 and 18-22 are being cancelled without prejudice or disclaimer. New claims 23-25 are being added.

All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

Claims 5, 7 and 20 were rejected under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement. As indicated, Claims 5, 7 and 20 are being cancelled without prejudice or disclaimer. The rejection thus becomes moot.

Prior Art Rejections

Claims 2-5, 7-13 and 18-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over US Patent No. 6,226,734 to Kleinsorge et al. (hereinafter "Kleinsorge") in view of in view US Patent No. 6,2763,519 to McColl et al. (hereinafter "McColl"), and claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over Kleinsorge and McColl in view of US Patent No. 6,279,098 to Bauman et al. (hereinafter "Bauman"). These rejections have been carefully considered, but are most respectfully traversed.

The computer system of the present invention (for example, the embodiment depicted in Fig. 1; p. 13, 3rd paragraph to p. 22, 1st paragraph), as recited in claim 23, comprises: one or more CPUs (10, 11, 12); a main memory 30; software means for logically dividing the computer system into a plurality of logical partitions 0-4 each of which includes a subset of the main memory 30 and a subset of CPUs that works independently from the remaining CPUs ("by space sharing" Abstract; p. 11, 1st full paragraph; Fig. 2C; p.22, 2nd paragraph; "*FIG. 16 is a flowchart of the process of shifting an space-shared I/O adapter from a partition to another in the computer of FIG. 1*") or under a time-sharing manner with the remaining CPUs ("by time

sharing" Abstract; Fig. 2B; p. 10, last paragraph; p.22, 2nd paragraph); and control means (20, 100, 101) including one or more input/output adaptors (100, 101), each of the adaptors being connected to an input/output device through an network 110 (via 100a), controlling outbound access of reading-out outbound data packets from said logical partitions, sending the outbound data packets to said input/output device, and controlling inbound access of writing inbound data packets, said inbound data packets being transmitted from said input/output device and stored in receive buffers 1700-1703 ("*FIG. 14 is an illustration of a receive buffer of the computer of FIG. 1*") provided individually for each of said logical partitions according to a destination of each inbound data packet, into said main memory 30.

Each of said input/output adaptors includes: a send/receive allocation register 150 for storing a value set indicating input/output performance allocation among said logical partitions as to the inbound/outbound access of said each input/output adaptor (Fig. 4; p. 19, last paragraph to p. 20, 2nd paragraph; "*A send/receive allocation register 150 regulates the allocation of I/O capacity among the partitions.*" P. 11, lines 4-6; "*FIG. 18 is an illustration of an example of set values of a setting file for booking allocation of I/O capacity among partitions in the computer of FIG. 1*"; "*The upper limit of the number "n" for each partition is held by the send/receive allocation register 150.*" P. 20, lines 6-7); a send scheduler 140 for switching a reading-out target from which the outbound data packets are read-out among said logical partitions, according to said value set stored in said send/receive allocation register 150 (p. 18, last paragraph to p. 20, 1st paragraph; "*FIG. 3 is a flowchart of the processing of a send scheduler of the computer of FIG. 1*"; "*When the I/O adapter 100 performs data I/O processing for a plurality of partitions, a send scheduler 140 and a receive scheduler 190 determine in what proportions the I/O adapter 100 should perform the data I/O processing for the partitions.*" P. 10, last line to p. 11, line 4); a receive scheduler 190 for switching a reading-out target from which the inbound data packets are read-out to write into said main memory 30 among said receive buffers 1700-1703, according to said value set stored in said send/receive allocation register 150 ("*FIG. 5 is a flowchart of the processing of a receive scheduler of the computer of FIG. 1*"; p.21, 1st paragraph).

As recited in claim 24, the send/receive allocation register 150 stores a number of outbound data packets to be consecutively read-out from each of the partitions, and said send scheduler 150 controls timings for shifting the reading-out target among the logical partitions, according to the stored number of the outbound data packets to be consecutively read-out ("*In the partition-control program, the ratio of I/O allocation for each partition is rounded to the simplest possible whole number (of an approximate value, if necessary), and the send/receive*

allocate register 150 is informed of the number of packets that each partition can continuously send and receive." P. 24, last paragraph).

As recited in claim 25, the send/receive allocation register 150 stores a number of inbound packets to be consecutively read-out from each of the receiving buffers 1700-1703 provided for each of the partitions, and said receive scheduler 190 controls a timing for shifting the reading-out target among the receiving buffers 1700-1703, according to the stored number of the inbound data packets to be consecutively read-out.

The invention allocates input/output performance of an I/O adapter among logical partitions. In other words, traffic of outbound data packets or inbound data packets provided by the I/O adapter is allocated among plural logical partitions. In particular, the input/output performance allocation among logical partitions is set in the send/receive allocation register 150, the send scheduler 140 controls switching of a reading-out target from which outbound data packets are read-out among logical partitions, and the receive scheduler 190 controls switching of reading-out target from which inbound data packets are read-out among receive buffers. The outbound data packets are physically read out from main memory 30 which is divided into the partitions. Accordingly, the invention reads out outbound data packets from said logical partitions to define outbound access of the I/O adapter (e.g., "*transmit a packet of data of the partition 0*" p. 19, lines 13 -16). According to the invention, through the scheduling by the send scheduler 140 and the receive scheduler 190, the total input/output performance provided by the I/O adapter is allocated to logical partitions. The allocation ratio of the input/output performance to each logical partition can be set.

Applicants contend that none of the cited prior art references teaches or suggests "allocating one or more I/O adapters on a time sharing basis among logical partitions" or "the send scheduler 140 and the receive scheduler 190 for scheduling the total input/output performance by the I/O adapter allocated to logical partitions" according to the invention.

In contrast, Kleinsorge only provides a multiprocessor system in which system hardware is divided into logical partitions. The I/O processor 118 is shared by the logical partitions. Kleinsorge is simply silent about any mechanism to prescribe/set and to control allocation of input/output performance provided by an I/O adapter among logical partitions on a time sharing basis as in the present invention.

Further, Kleinsorge fails to provide the send scheduler 140 and the receive scheduler 190 of the present invention to schedule the total input/output performance by the I/O adapter allocated to logical partitions. As such, the present invention can set an allocation ratio of the input/output performance to each logical partition. Kleinsorge fails to disclose such an

input/output performance allocation control.

McColl and Bauman fail to compensate for the deficiencies of Kleinsorge.

Applicants contend that the cited references or their combinations fail to teach or disclose each and every feature of the present invention as disclosed in the independent claim 23. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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